Fraunhofer
EMFT

Master's Thesis:

Design of a sub 1 V Bandgap Refence Circuit in FD-SOI CMOS Technology

Job location: Munich
Duration: min. 6 Months

The Fraunhofer EMFT works on the research and development of technologies and solutions in the field of microelectronics and microsystems technology. It takes an interdisciplinary approach, combining traditional silicon semiconductor technologies with MEMS, microfluidics, system integration and flexible electronics. The focus here is not on miniaturization alone, but primarily on the heterogeneous technology integration and development of intelligent systems to enable novel solutions and products for everyday use.

Project:
The research project THINGS2DO (Abbreviation for: „Thin but great Silicon to Design Objects") aims to establish a sustainable ecosystem for the realization of semiconductor components, based on the FD-SOI (Fully Depleted Silicon on Insulator) technology, in Europe. The project will allow small and medium-sized companies as well as large-scale industry and research to combine, integrate and produce IP-components and system solutions based on advanced FDSOI technology (on-chip elements like Central Processing Unit, image processors, memory chips, I/O-modules, voltage generators, A/D converter or PLL).

Goal of the Master's Thesis:
A bandgap reference (BGR) is an indispensable component in integrated circuits (ICs) like in DRAM, ADC, DAC, and smart temperature sensors. It provides reference voltages and currents that are to a large extent robust against variations in process parameters, supply and temperature. The BGR functions on the principle of adding 2 voltages- one with positive temperature coefficient and another that has a negative temperature coefficient. The conventional BGR output voltage is around 1.25 V that is close the bandgap voltage of Silicon. This limits the scaling down of their operating voltage. However, BGR capable of sub 1 V operation is essential for designing ICs operating at low supply voltages. The tasks for this master's thesis position are:

- Evaluation of different design concepts for sub 1 V Bandgap references.
- Design, layout and verification of the Bandgap refence circuit
- Documentation and presentation of the results.

For questions regarding the position please do not hesitate to contact:

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